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(12) # EUROPEAN PATENT APPLICATION

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(54) **Method of mounting a carrier for a microelectronic silicon chip.**

(57) A chip carrier (11) is to be mounted on a substrate (13) which includes a thermally conductive layer (14). A hole is formed in an insulating layer (15) to expose the thermally conductive layer (14) and the hole is filled with a thermally conductive material (18). A metallised zone (20) of the carrier overlays the material (18) and is soldered thereto with the same solder as is used to make electrical connections (12, 17, 19) to the carrier (11).

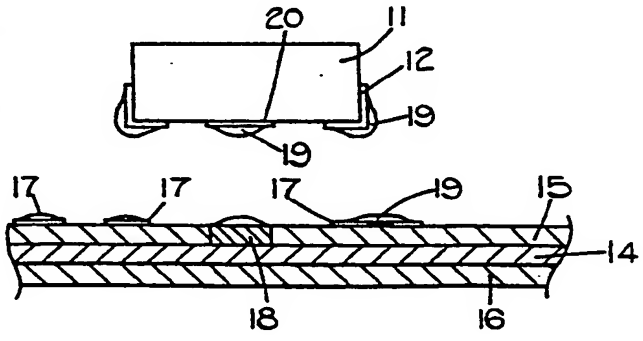

FIG.2.

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METHOD OF MOUNTING A CARRIER FOR A MICROELECTRONIC SILICON CHIP

This invention relates to a method of mounting, onto a substrate a carrier for a microelectronic silicon chip.

Silicon chips are frequently mounted in chip carriers which are provided with terminal pads instead of external leads and are commonly known as leadless chip carriers, permitting increased packing density of the carriers on a printed circuit board.

Such chip carriers are typically square and are provided on all four sides with terminal pads which are electrically connected to conductors on a printed wiring board. The high packing densities obtainable with these components necessitate good thermal contact with a thermally conductive element on the printed wiring board. It is known to include a thermally conductive layer within the printed wiring board and to provide a thermally conductive paste, rubber or plastics material between the underside of each chip carrier and either the surface of the board or the thermally conductive layer, the latter being effected by local removal of an insulating layer of the board. Such an arrangement is liable to result in stress being applied to soldered joints between terminal pads and printed wiring conductors, as a result of differential thermal expansion between the solder and interposed thermally conductive material, in a direction normal to the plane of the board.

It is an object of the invention to provide a method of reducing the thermal resistance between a silicon chip carrier and a supporting substrate, such that stresses due to differential expansion are reduced.

According to the invention there is provided a method of mounting a carrier of a microelectronic silicon chip on to an electrically insulating support which includes a layer of high thermal conductivity, said method including the steps of making a thermal connection between said layer and an electrically insulating surface of said support at a location thereon where said carrier is to be secured, metallising a zone of a face of said carrier which is to lie adjacent said support, and soldering said metallised zone to said thermal connection.

Embodiments of the invention will now be described by way of example only and with reference to the accompanying drawings in which:-

Figure 1 is a plan view of a micro-chip carrier;

Figure 2 shows, somewhat diagrammatically, an intermediate stage in attaching a chip carrier to a printed wiring board;

Figure 3 is a view, corresponding to Figure 2, showing the carrier attached to the board, and

Figure 4 shows an alternative method of making a thermal connection between a chip carrier and a multilayer substrate.

As shown in Figure 1 an electronic micro-chip, indicated at 10, is mounted within a carrier 11 which is square in plan view and which has on each of its sides terminals 12 for leads (not shown) from the chip 10.

As shown in Figures 2 and 3 a printed wiring board 13 comprises a thermally conductive layer 14 which is sandwiched between two electrically insulating layers 15, 16. The outer surface of the layer 15 is provided, by any known means, with patterns of wiring 17 for providing interconnections between the terminals 12 and external connections or corresponding terminals on other chip carriers.

A portion of the layer 15 is removed, by boring or other suitable means, at a location which corresponds to the centre of a carrier 11 to be mounted on the board 13. The board 13 is then electro-plated, for example with copper, to provide a thermally conductive pad 18 between the layer 14 and the exposed surface of the layer 15. The underside of the carrier 11, adjacent the chip 10 is provided with a metallised zone 20, for example by vacuum deposition, plating or spraying, comprising successive layers of nickel-chrome alloy, nickel and gold. The terminals 12, the zone 20, the wiring 17 and the pad 18 are pre-coated with identical solder, as indicated at 19 in Figure 2. The carrier 11 is then located in its required position on the board 13 and the temperature is raised to that of melting point of the solder. Surface tension of the solder pulls the carrier 11 accurately into its required position on the board 13, as shown in Figure 3.

It will be understood that the board 13 could be a known type of double sided printed wiring board.

It will also be understood that the board 13 could alternatively comprise known type of multilayer substrate having a large number of wiring interconnections at different levels and provided with outer insulating layers corresponding to the layer 15 described above, one or both of the outer layers covering a thermally conductive layer corresponding to the layer 14.

Such an board 30 is shown in Figure 4 and comprises a multilayer substrate 31 of a known type which includes a plurality of insulating layers provided with through conductors known as "vias", and with embedded conductive connections, the vias passing between the substrate layers to contact selected ones of the aforesaid conductive connections, so as to provide required electrical connections between chip carriers or other components on both sides of the assembly. The substrate 31 is coated on both sides with insulating adhesive layers 33 and over these are located molybdenum sheets 34 having a high thermal conductivity and provided with apertures 35 at locations adjacent those where it has previously been determined that terminals of chip carriers will be positioned. Copper foil-clad insulating sheets 36 are adhesively mounted on the sheets 34, and the layers are pressed together to effect bonding and to cause the insulating adhesive 33 to flow into the apertures 35.

Holes 37 are drilled right through the boards 30 at required locations of the terminals 38 of chip carriers, only one such carrier being shown at 39.

The positions of the vias and/or the connections in the substrate 31 will have been designed so that the holes 37 will enable the necessary interconnections to be made between chip carriers and other components on the assembly.

Additionally a plurality of holes 40 are drilled through the board 30 to expose the molybdenum sheets 34 at locations which will lie under the bodies of the chip carriers 39. The copper foil on the sheets 36 and the insides of the holes 37, 40 are plated with copper 45 by the well-known through-plating technique. The plated foil layers are then etched, by known means, to provide a pattern of conductive lands 41 to which the terminals 38 of the carriers 39 are to be soldered, and to leave lands 42 around each group of holes 40.

Solder 43 is applied to the lands 41, 42 and preferably is allowed to pass into the holes 37, 40 by capillary action. The undersides of the carriers 39 are each provided with a metallized zone 44, as described above with reference to the first embodiment, and the same solder 43 is also applied to the zone 44 and the terminals 38. The carriers 39 are then located on the lands 41, 42 and the solder 43 is briefly reliquidised to complete the assembly.

CLAIMS

1. A method of mounting a carrier (11 or 37) of a microelectronic silicon chip on to an electrically insulating support (13 or 30) which includes a layer (14 or 34) of high thermal conductivity, said method including the steps of making a thermal connection (18 or 45) between said layer (14 or 34) and an electrically insulating surface (15 or 36) of said support (13 or 30) at a location thereon where said carrier (11 or 39) is to be secured, metallising a zone (20 or 44) of a face of said carrier (11 or 39) which is to lie adjacent said support (13 or 30) and securing said zone (20 or 44) to said thermal connection (18 or 45) by means of a thermally conductive material (19 or 43), characterised in that said zone (20 or 44) is secured to said thermal connection (18 or 45) by means of the solder which is used to secure terminals (12 or 38) of the carrier (11 or 39) to a wiring pattern on the support (13 or 30).

2. A method as claimed in claim 1 in which said thermal connection is made by forming a hole in said insulating surface (15 or 36) to expose said layer (14 or 34) of high thermal conductivity, and introducinga thermally conductive material (18 or 45) into said hole.

3. A method as claimed in claim 2 in which said introduction of thermally conductive material (45) into said hole (40) is effected by plating.

4. A method as claimed in claim 2 or claim 3 in which solder (43) is introduced into said hole (40).

5. A method as claimed in claim 2 or claim 3 in which a plurality of said holes (40) are formed and a thermally conductive material (45) is introduced into each.

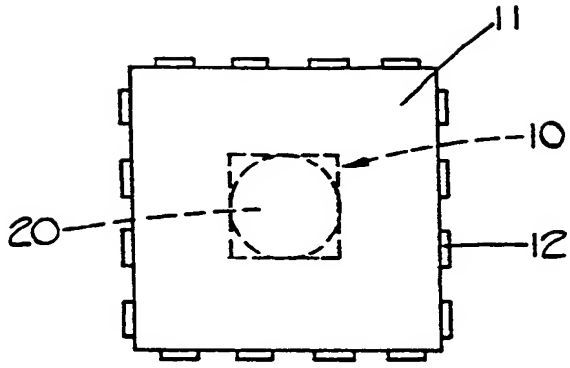

FIG.1.

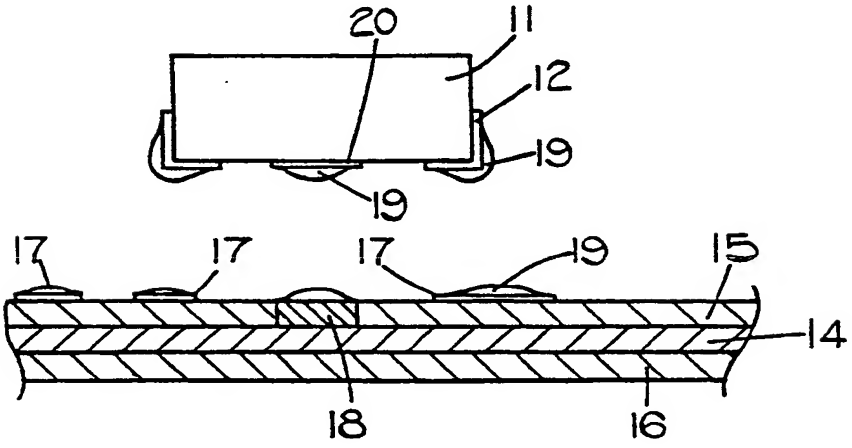

FIG.2.

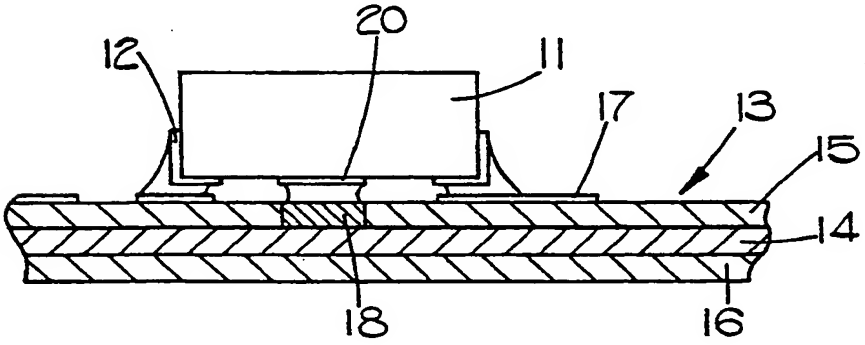

FIG.3.

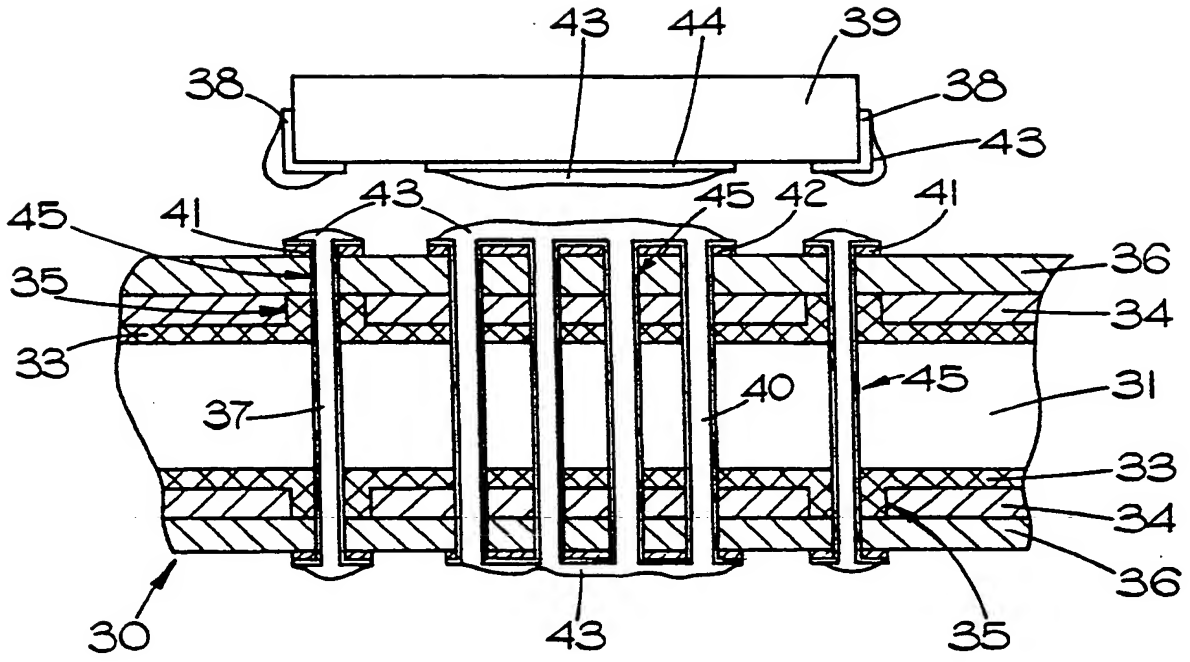
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FIG. 4.

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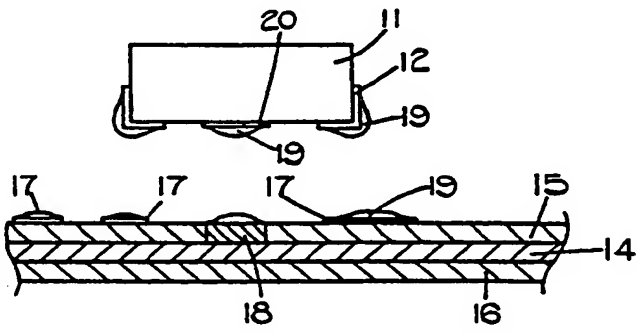

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EUROPEAN SEARCH REPORT

0139431
Application number

EP 84306014.6

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.⁴)
A	US - A - 3 486 223 (BUTERA) * Fig. 1,3-5; abstract * --	1	H 05 K 3/34 H 01 L 23/36
A	US - A - 3 921 285 (KRALL) * Abstract; fig. 1-5 * --	1	
A	US - A - 4 164 811 (HEYWANG) * Abstract; fig. 1,2 * --	1	
A	CH - A5 - 614 810 (IBM) * Abstract; fig. 1-7 * --	1	
A	DE - A1 - 3 042 085 (HITACHI) * Fig. 3,4,6,7 * ----	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.⁴)

H 05 K 3/00
H 01 L 21/00
H 01 L 23/00
H 01 R 4/00
H 01 R 43/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	19-02-1985	VAKIL

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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